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(54) Name of Invention: Method of Manufacturing Semiconductor Device

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Specifications

1. **Name of Invention:** Method of Manufacturing Semiconductor Device

2. **Scope of Patent Application**

(1) In a method for manufacturing a semiconductor device that includes an insulated-gate field-effect transistor, a semiconductor manufacturing method which is characterized by including --

- a process that forms the gate electrode of the aforementioned insulated-gate field effect transistor,

  a process that forms an oxide film on the entire surface,
- a process that selectively forms a diffusion layer with a low impurity concentration, using the above-noted gate electrode as a mask,
- a process that forms and processes a silicate glass film consisting of phosphor-silicate glass or phosphor-silicate glass containing boron, and
- a process that dry-etches the entire surface of the above-noted silicate glass film to leave said silicate glass film only on the side surfaces of the above-noted gate electrode and so forms its sidewalls. *

(2) A manufacturing method for the semiconductor device described in Scope of Patent Application Item (1) in which the phosphorus concentration in the phosphor-silicate glass is 10 mole-percent or more, the boron concentration of the boron-containing phosphor-silicate glass is 5~15 mole-percent and phosphorus concentration is 4~10 mole-percent.

3. Detailed Explanation of Invention

Field for Commercial Utilization: This invention is one bearing on a method of manufacturing a semiconductor device that includes an insulated-gate type field effect transistor having an LDD (lightly doped drain) structure.

Usual Technology With the short-channeling of insulated-gate field-effect transistors (hereafter, MIS [metal-insulated semiconductor] transistors), hot carriers become easily injected into gate oxide film since the drain field has become higher, and so seriously degrade the traits. Especially noticeable are such trait fluctuations as in gm or N-channel MIS transistors' path-value [?? word not fully legible -- Translator] voltages due to hot electron injection. The LDD structure is one typical of ways for modifying a drain field by the device's structure and so reducing hot carrier injections.

Figures 2(a) and (b) are schematic cross-sectional diagrams to illustrate an example of the method of manufacturing the usual semiconductor device having an MIS transistor with an LDD structure. As shown in Figure 2(a), after making an n^- layer as a low-concentration diffusion layer, one uses CVD and RIE (reactive ion etching) to leave oxide film on gate electrode 3's side surfaces to form CVD-oxidized sidealls 5.

*[Bullets added by translator for ease of reading.]

Next, one forms n^+ layer 6 as a high-concentration diffusion layer, as shown in Figure 2(b). Her, one keeps n^- layer 4's voltage low between the effective source and drain so as to suppress hot-carrier injection into gate oxide film 10. In Figures 2(a) and (b), 1 is a P-type silicon substrate, 2 is a field oxide film and 9 is a thermal-oxide film.

Problems the Invention Seeks to Resolve

In this usual example of an LDD structure, the formatting of CVD-oxidized sidewall 5 must be done with extra RIE, considering the thickness variations in the CVD oxidized film on the [word illegible] and variations in intra-wafer etching by RIE. However, with over-etching the substrate will be etched in the source and drain regions and become the cause of source/drain junction leaks. Short-channeling of an MIS transistor is a problem in having junction leaks occur more easily the shallower the junction is.

So, this invention's aim is to resolve the above problems by providing a method of manufacturing a semiconductor device that includes forming sidewalls on its gate electrode so that the transistor traits will not degrade even if over-etched by RIE, and includes an MIS transistor with the LDD structure.

Means to Resolve the Problems: In a method for fabricating a semiconductor device containing an insulated-gate field effect transistor, this invention's method of manufacturing a semiconductor device has a process to form a gate electrode of the above-noted MIS field-effect transistor, a process to form an oxide film over the entire surface, a process to selectively form a diffusion layer with a low concentration of impurity, using the above-noted gate electrode as a mask, a process to form and heat-process a silicate glass film consisting of phosphor-silicate glass or phosphor-silicate glass containing boron, and a process to dry etch the entire surface of the above-noted silicate glass film so as to leave it only on the side surfaces of the above-noted gate electrode as a sidewall.

Application Example

Below I will explain an application example of this invention while referring to the figures.

Figures 1(a)~(d) is a schematic cross-sectional diagram of the device to explain one application example of this invention.

As in Fig. 1(a), on P-type silicon substrate 1 one uses normal methods to form field oxidized film 2 and oxidized gate film 10, to form gate electrode 3 by patterning, e.g., a polysilicon layer, and also forms thermal-oxide film 9 over the entire surface. After that one uses ion-injection with gate electrode 3 as a mask to form n^- film 4 as a diffusion layer with a low impurity concentration. Next one forms PSG (phosphor-silicate glass) film 7 containing a high phosphorus concentration, e.g., 10 mole-percent or more.

Usually, instead of PSG film 7 with its high phosphorus concentration, a CVD-oxidized film is used, as shown in Figures 2(a)and (b); but the enroachment (overhang) of a CVD-oxidized film such as shown in Figure 1(a) can intrude on the sides of gate electrode 3. Such overhang will become a big problem if the sidewalls are very narrow. On the other hand, with high-phosphorus PSG film the same kind of overhang is seen after film deposition as with CVD-oxidized film. But after the PSG film is deposited, one can do thermal treatment. for instance 5~10 minutes in a steam environment at 800~900°C as shown in Figure 1(b) to make PSG film 7 sag and fully embed the above-noted overhang.

Next, as shown in Fig. 1(c), one etches the entire surface by RIE to form PSG sidewalls 8. Since a high concentration of phosphorus is now contained in PSG film 7, one can make the niching selectivity ratio of thermal-oxide film 9 some 1:4 to 1:5 by choosing the dry etching conditions. The higher the phosphorus concentration in PSG film 7, the higher one can make the selectivity ratio. Also, when using the usual CVD-oxidized film as a sidewall, whereas the selectivity ratio with underlying thermal-oxide film 9 is nearly 1:1, it is 1:4 to 1:5 with PSG film 7. So, no damage is done to the surface of the underlying silicon substrate by over-etching, nor are junction leaks to be seen.

Then, as shown in Fig. 1(d), one forms n^+ layer 6 as a high-concentration diffusion layer. Next one successively forms the element separator film [? Assumed from unclear word--Translator], a contact hole and electrode.

PSG sidewall 8, with its high phosphorus concentration, has a marked porosity, so that it is desirable to remove it after forming n^+ layer 6. If an etching solution made up of $HF:H_2O$ = a ratio of 1:50 or 1:60 is used for removal by etching, one can make the etching rate of underlying thermal-oxide film 9 to PSG sidewalls 8 1:50 or 1:60 and so can remove just PSG sidewalls 8 with scarcely any reduction in the thickness of field oxide film 2, et al.

In the above application example I used PSG film; but the same effects can be obtained also by using boro-phosphor-silicate glass (BPSG) with a boron concentration of 5~15 mole-percent and phosphorus concentration of 4~10 mole-percent.

Effectiveness of Invention: As explained above in detail, this invention employs the above means by which one can manufacture a high-throughput, high-reliability semi-conductor device which contains an insulated-gate field-effect transistor with an LDD structure and little occurrence of junction leaks.

4. Simple Explanation of Figures

Figures 1(a)~(d) and 2(a) and (b) are respectively schematic cross-sectional diagrams to explain the fabrication of one application example of this invention and of the usual case.

1 ... P-type silicon substrate
2 ... Field oxide film
3 ... Gate electrode
4 ... n^- layer
5 ... CVD-oxidized film sidewalls
6 ... n^+ layer
7 ... PSG film
8 ... PSG film sidewalls
9 ... Thermal-oxide film
10 ... Gate oxidized film

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